REMARKS

In the present Office Action, claims 1 - 12 were examined. Claims 1 - 12 are rejected. No claims are presently objected to or allowed. By this Amendment, claims 2 and 8-10 have been amended, no claims have been canceled and no claims have been added. Accordingly, claims 1 - 12 are presented for further examination. No new matter has been added. By this Amendment, claims 1 - 12 are believed to be in condition for allowance.

The Examiner requested restriction between the claims of Group I, claims 1-12 drawn to a device and the claims of group II, claims 13-20, drawn to a method of making that device. During a telephone conversation with Applicants' attorney on July 24, 2007, a provisional election was made to prosecute the claims of Group I, claims 1-12 with traverse. Applicants confirm the election of Group I in traverse as follows:

The Group I claims are drawn to a package of encasing semiconductor devices having a lead frame that terminates in an array of lands. A first molding compound is disposed between the individual lands. A second molding compound encapsulates the semiconductor device. Claim 13 is drawn to a method for the manufacture of substrate package that includes forming an electrically conductive substrate to form an array of lands and disposing a first molding compound between the individual lands. A second molding compound is then used to encapsulate the at least one semiconductor device. So while the claims of Group I and the claims of Group II are patently distinct, both relate to semiconductor packages having two molding resins applied to different parts of the package. The two groups of claims are sufficiently interrelated that an examination of one group of claims would require an examination of class/subclass designations required to search the other group. Therefore, the Examiner would not be unduly burdened to search both groups of claims at the same time. It is respectfully requested that the restriction requirement be removed and all claims fully examined on their merits.

In the event that the Examiner repeats the restriction requirement and makes it Final, Applicants reaffirm the election of the claims of Group I, claims 1-12.

Two amendments have been made to clarify the specification. Paragraph [0003] has been amended to correct a grammar error. Paragraph [0010] has been amended to update the status of a commonly owned U.S. patent application that is now granted as a patent.

Applicants' invention, as illustrated in Figure 8, is drawn to a package encapsulating a semiconductor device where the device is directly electrically interconnected to input/output pads of the device and, in some embodiments, passives or other components are also encapsulated.. As disclosed in Applicants' specification at page 7, line 13, by directly it is meant that the interconnection is by a flip chip method without the use of an intervening wire bond or tape automated bonding (TAB) tape. Further, there is a first molding compound disposed between individual lands of the array of lands and a second molding compound encapsulating the semiconductor device. In accordance with Applicants' claim 2, the lead frame and routing circuits interconnecting the array of lands at one end of the lead frame and chip attach sites at the other end of the lead frame are all formed from a single electrically conducted substrate. This is in accord with Applicants' specification at page 1, line 14. While Applicants believe that the expression "monolithic" as originally presented in claim 2 conveys the same structure, this amendment has been made to more precisely claim the single electrically conductive material of the lead frame and routing circuits. Claims 8-10 have been amended to remove a multiple dependency and to replace the word monolithic in conformance with the amendment to claim 2.

Applicant's claims 1-5 and 9-12 were rejected under 35 U.S.C. 103(a) as unpatentable over *Bayan, et al.* (U.S. Patent 6,664,615) in view of *Brodsky* (U.S. Patent 6,670,222). With reference to Figure 7B of U.S 6,664,615, *Bayan, et al.* disclose a semiconductor device in which the die terminals (i.e., input/output pads) 670 are electrically connected by bond wires 680 (U.S. 6,664,615 at column 5, lines 5-6) and not directly electrically interconnected as recited in Applicants' Claim 1 and defined in Applicants' specification at Page 7, line 13. *Bayan et al.* dispose a non-conductive ('615 Patent at column 5, line9) die attach material 710 between the semiconductor device and the leadframe teaching away from (in fact preventing) direct electrical interconnection. As such, *Bayan et al.* do not teach nor suggest direct electrical interconnection of a lead frame to input/output pads on the semiconductor device as recited in Applicants' Claim 1.

U.S. 6,670,222 discloses a textured die pad to enhance adhesion of a polymer die attach to a backside of a semiconductor device. As shown in U.S. 6,670,222, wire bonds 102 are used to electrically interconnect input/output pads on the semiconductor device to a lead frame. Accordingly, there is nothing in either of U.S. 6,664,615 and 6,670,222 to teach or suggest a package as claimed by Applicants with direct electrical interconnection between input/output pads of a semiconductor device and lead frames terminating in an array of lands with a first molding compound between that array of lands and a second molding compound encapsulating the semiconductor device. As such, the combination neither teaches nor suggests Applicants' invention and Applicants' claims 1-12 should be allowed over the combination of references.

Claims 2 and 8 have been amended to more precisely identify that the combination of array of lands, routing circuits and chip attached sites are formed from a single electrically conductive substrate. Both U.S. 6,664,615 and 6,670,222 have multiple electrically interconnected components to deliver an electrical signal from input/output pads on the semiconductor device and lands adapted to be bonded to external circuitry. Applicants' claims 1, 2 and 8 and the claims dependent therefrom should be allowed over the combination of references.

Claims 3-7 and 9-12 depend from and further limit and define one of claims 1, 2 and 8. As these claims are now believed to be in condition for allowance, the dependent claims should likewise be allowed.

Accordingly, Applicants submit that none of the references, alone or in combination, anticipate or make obvious the invention as presently claimed and that the application is now in condition for allowance. Therefore, Applicants respectfully request reconsideration and further examination of the application and the Examiner is respectfully requested to take such proper actions so that a patent will issue herefrom as soon as possible.

If the Examiner has any questions or believes that a discussion with Applicant's attorney would expedite prosecution, the Examiner is invited and encouraged to contact the undersigned at the telephone number below.

Please apply any credits or charge any deficiencies to our Deposit Account No. 23-1665.

Respectfully submitted,
Shafidul Islam, et al.

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